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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/751,750	12/29/2000	Talal K. Jaber	2207/10083	5033

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EXAMINER	
LAMARRE, GUY J	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 01/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/751,750	JABER	
	Examiner	Art Unit	
	Guy J. Lamarre, P.E.	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 July 2004* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-11 and 13-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3-11, 13-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

FINAL OFFICE ACTION

0. This office action is in response to Applicants' Amendment of 12 July 2004.

0.1 **Claims 1, 3-4, 6, 9, 11, 13-14, 16, 19** are amended, **Claims 2, 12** are cancelled. **Claims 1, 3-11, 13-20** remain pending.

0.2 The prior art rejections of record are maintained in response to Applicants' Amendments.

Response to Arguments

0.3 Applicants' arguments have been fully considered, but they are not found persuasive.

REMARKS

1. In response to **Claims 1, 3-11, 13-20**, Applicants argue, on page 7 para. 2 et seq., that the prior art of record does not teach the claimed invention, i.e., test weighting/biasing with register means and channel filtering logic that masks out unwanted test results from tested channels to prevent such from appearing as input to be compressed in MISR or to other devices.

Examiner disagrees and notes that the prior art of record, namely **Motika et al.**, does disclose equivalent test weighting/biasing with register means in Fig. 4 wherein *Numeral 12* generates test data that is applied to WRP 144 to be biased/weighed as described in col. 5 line 3 et seq. and col. 6 line 3 et seq., said biasing being effected selectively on the plural applied test bits from *Numeral 12*. See Fig. 4 *Numeral 144* for additional weight distribution forced onto output of *Numeral 12* with related register/storage means.

Examiner further notes that the prior art of record, namely **Rajski et al.**, does disclose equivalent channel filtering logic along with test response masking means in Fig. 14: *Block 176*(as reproduced below at page 5 of instant final rejection), wherein a channel selecting/filtering logic masks undesired test responses or undesired bits of the test responses. Subsequently, desired test responses are passed to be compressed via MISR in Block 178.

Therefore, said claims are not distinguished over the prior art of record.

1.1 To the extent that the response to the applicant's arguments may have mentioned new portions of the prior art references which were not used in the prior office action, this does not constitute a new ground of rejection. It is clear that the prior art reference is of record and has been considered entirely by applicant. See *In re Boyer*, 363 F.2d 455, 458 n.2, 150 USPQ 441, 444, n.2 (CCPA 1966) and *In re Bush*, 296 F.2d 491, 496, 131 USPQ 263, 267 (CCPA 1961).

The mere fact that additional portions of the same reference may have been mentioned or relied upon does not constitute new ground of rejection. *In re Meinhardt*, 392, F.2d 273, 280, 157 USPQ 270, 275 (CCPA 1968).

Claim Rejections - 35 USC ' 102

2.1 Claims 1, 3-8 and 11, 13-18 are rejected under 35 U.S.C. 102 (b) as being anticipated by **Motika et al.** (US Patent No. 5,983,380; 9 Nov. 1999 (issue date)).

Motika et al. discloses IC configurations having logic circuits and self-test circuits wherein plural testing schemes are employed to reduce testing time, save energy and minimize circuit complexity.

As per Claims 1, 11, Motika et al. depicts, e.g., in Fig. 6 and related description in col. 1 line 25 et seq., the claimed on-chip testing apparatus comprising: a test pattern generator (Fig. 6 Numeral 12, col. 2 line 35) to generate test data for a plurality of testing channels; and a weight selector (Fig. 6 Numerals 118-126 with Numerals 138 and 142, Fig. 5, col. 2 line 35) coupled to said test pattern generator, said weight selector to store weighting values to bias data (e.g., col. 2 line 62) for at least one of said testing channels.

Motika et al. depicts, in Fig. 6 and related description in col. 2 line 25 et seq., the claimed apparatus wherein said weight selector includes a weight storage register (Fig. 6 Numerals 118-126 with Numerals 138 and 142, Fig. 5, col. 2 line 35) to store said weighting

values and said weight selector is to selectively bias data (e.g., col. 2 line 62) individual bits of said test data.

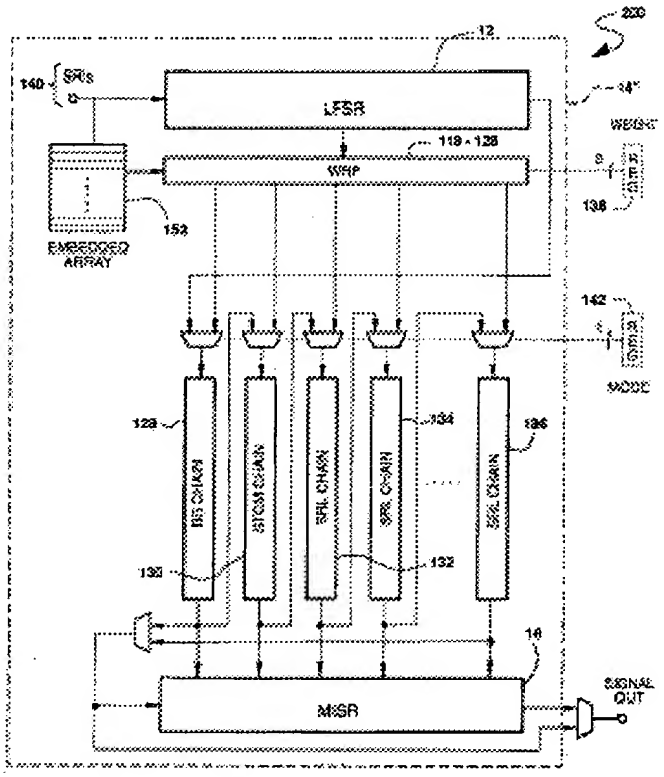


FIG - 6

As per Claims 3, 13, Motika et al. depicts, in Fig. 6 and related description in col. 2 line 25 et seq., the claimed apparatus wherein said weight selector (Fig. 6 Numerals 118-126 with Numerals 138 and 142, Fig. 5, col. 2 line 35) causes a reduction in power usage when said weight storage registers store weighting values to bias (e.g., col. 2 lines 60-62: number of patterns is reduced resulting in power savings) data for at least one testing channels to one of all 0 values and all 1 values.

As per Claims 4, 14, Motika et al. depicts, in Fig. 6 and related description in col. 2 line 25 et seq., the claimed on-chip testing apparatus comprising: a test pattern generator (Fig. 6 Numeral 12, col. 2 line 35) to generate test data for a plurality of testing channels; clock control logic (e.g., col. 5 line 1 et seq., col. 6 line 38, loading or scanning at appropriate clocks and

associated implementation logic) to selectively supply scan clocking signals to said testing channels, such that said scan clocking signals scan said test data into said testing channels.

As per Claims 5, 15, Motika et al. depicts, in Fig. 6 and related description in col. 2 line 25 et seq., the claimed apparatus further comprising: a signature register (Fig. 6 Numeral 16, col. 2 line 65) coupled to said testing channels to receive data from said testing channels when said scan clocking signals are supplied to said testing channels.

As per Claims 6, 16, Motika et al. depicts, in Fig. 6 and related description in col. 2 line 25, the claimed on-chip testing apparatus comprising: clock control logic (e.g., col. 5 line 1 et seq., col. 6 line 38, loading or scanning at appropriate clocks and associated implementation logic) to selectively supply functional clocking signals to a plurality of testing channels, such that said functional clocking signals operate logic in said testing channels.

As per Claims 7, 17, Motika et al. depicts, in Fig. 6 and related description in col. 2 line 25 et seq., the claimed apparatus wherein said clock control logic further includes clock control logic to generate stop clock signals to said testing channels in e.g., col. 2 lines 10-25, col. 5 line 1 et seq., col. 6 line 38, loading or scanning at appropriate clocks and associated implementation logic.

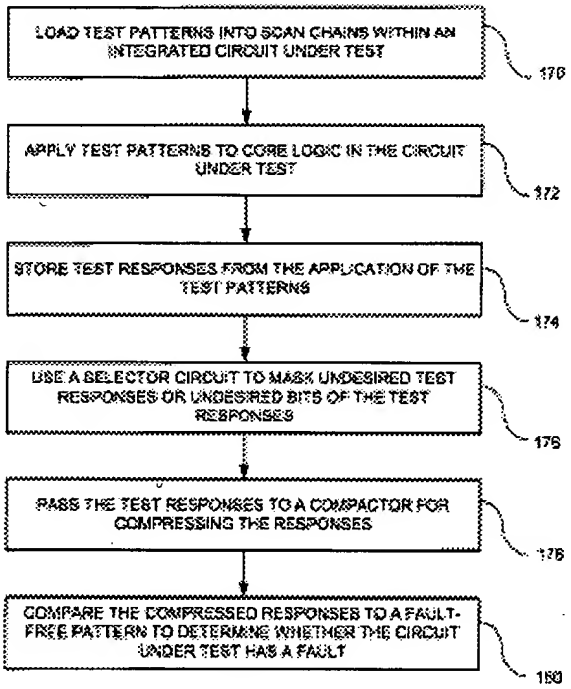
As per Claims 8, 18, Motika et al. depicts, in Fig. 6 and related description in col. 2 line 25 et seq., the claimed apparatus wherein said clock control logic further includes a scan counter counting said functional clocking signals and a breakpoint stop register to store a value such that at least one of said stop clock signals is generated when a count in said scan counter matches a value in said breakpoint stop register in e.g., col. 2 lines 10-25, col. 5 line 1 et seq., col. 6 line 38, loading or scanning at appropriate clocks and associated implementation logic.

2.2 Claims 6-8, 9-10, 16-18, 19-20 are rejected under 35 U.S.C. 102 (e) as being anticipated by **Rajski et al.** (US Patent No. 6,557,129; filed: 23 Nov. 1999).

As per Claims 6-8, 16-18, Rajski's Fig. 8 anticipates such claims because provided are means to delay reading of output compaction data as described in col. 3 line 5 et seq.

As per Claims 9-10, 19-20, Rajski's Fig. 6 anticipates such claims because *scan chains 44* are effectively blocked or masked via control *block 46* prior to compaction by *block 48*. Also refer to Fig. 10 for logic implementation and also to col. 3 line 12, col. 13 lines 41-49 and col. 7 line 41 et seq., and MISR in Fig. 2: Block 22. Also see Fig. 14: Block 176.

FIG. 14



Claim Rejections - 35 USC ' 103

3. **Claims 9-10, 19-20** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Motika et al.** (US Patent No. 5,983,380; 9 Nov. 1999) in view of **Rajski et al.** (US Patent No. 6,557,129; 23 Nov. 1999).

As per Claims 9, 19, Motika et al. substantially depicts, in Fig. 6 and related description in col. 2 line 25, the claimed on-chip testing apparatus comprising: channel filtering logic to receive data from a plurality of testing channels, said channel filtering logic to select or mask output data from a selected testing channel, e.g., in Fig. 6: MUX receives inputs from left-most

BS chain and right-most SRL chain to effect selection control to MISR. **Not specifically described** in detail in **Motika et al.** is the step of output data masking. **However Rajski et al.,** in an analogous art, discloses a testing methodology wherein such techniques are described. {See **Rajski et al.,** Id., e.g., Fig. 14: Block 176 (above) and related description} **Therefore**, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the procedure in **Motika et al.** by including therein output data masking means as taught by **Rajski et al.,** because such modification would provide the procedure disclosed in **Motika et al.** with a technique wherein "undesirable test output data is concealed." {See **Rajski et al.,** col. 4 lines 43-47.}

As per Claims 10, 20, Motika et al. depicts, in Fig. 6 and related description in col. 2 line 25 et seq., the claimed apparatus further comprising: a signature register coupled to said channel filtering logic to receive said data e.g., in Fig. 6: MUX receives inputs from left-most BS chain and right-most SRL chain to effect selection control to MISR.

3.1 Claims 6-8, 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Applicants' Admitted prior art** (hereinafter **Admitted prior** art) in view of **Swoboda et al.** (US Patent No. 6,349,392; Filed: 14 July 1999).

As per Claims 6-8, 16-18, Admitted prior art substantially discloses the claimed the claimed on-chip testing means comprising: clock control logic (e.g., page 1 line 12 for loading or scanning at appropriate clocks and associated implementation logic) to selectively supply functional clocking signals to a plurality of testing channels (e.g., page 1 line 11) such that said functional clocking signals operate logic in said testing channels. {See **Admitted prior art,** page 1 para. 2 – page 2 para. 1, in passim, wherein on-chip testing apparatus and method are described.} **Not specifically described** in detail in **Admitted prior art** is the step of clock stopping means along with associated hardware for implementation thereof. However **Swoboda et al.,** in an analogous art, discloses a testing methodology in "*Devices, systems and methods for*

mode driven stops," wherein such techniques are described. {See **Swoboda et al.,** Id., e.g., Fig. 58 and in col. 14 lines 14-27 et seq., "*Connected to each test port is mode conditioned stop logic circuitry 1309S, 1309C and 1309A in the domains respectively. The modes are established by a mode register 1311 which is scanable in FIGS. 54 and 57 to establish the type of stop and any other desired mode characteristics for the domains. The mode conditioned stop logic circuits 1309S, 1309C and 1309A are respectively fed by MPSD decoders 1313S, 1313C and 1313A that have multiline outputs to the stop mode conditioned logic circuitry,*" register or storing or breakpoint means in col. 14 line 14} **Therefore**, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the procedure in the **Admitted prior art** by including therein clock stopping means as taught by **Swoboda et al.,** because such modification would provide the procedure disclosed in **Admitted prior art** with a technique wherein "*Data and control information are scanned into and out of the domains on test clock JCLK, and the domains are independently and selectively started on functional clock FCLK and stopped, in extensive sequences to accomplish emulation, simulation and test functions with a wide degree of flexibility as circumstances of the development, manufacturing and field environments dictate.*" {See **Swoboda et al.,** col. 20 line 9 et seq.}

Conclusion

4. THIS ACTION IS MADE FINAL. See MPEP § 609(B)(2)(i). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

4.1 Any response to this action should be mailed to:

Commissioner of Patents and Trademarks, Washington, D.C. 20231

or faxed to: (703) 872-9306 for all formal communications.

Hand-delivered responses should be brought to Customer Services, 220 20th Street S., Crystal Plaza II, Lobby, Room 1B03, Arlington, VA 22202.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Guy J. Lamarre, P.E., whose telephone number is (571) 272-3826. The examiner can normally be reached on Monday to Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert De Cady, can be reached at (571) 272-3819.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-3609.

Information regarding the status of an application may also be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Guy J. Lamarre, P.E
Primary Examiner
1/9/05